Analytical modeling of reservoir effect on electromigration in Cu interconnects

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Electromigration (EM) in Cu dual-damascene interconnects with extensions (also described as overhangs or reservoirs) ranging from 0 to 120 nm in the upper metal (M2) was investigated by an analytical model considering the work of electron wind and surface/interface energy. It was found that there exists a critical extension length beyond which increasing extension lengths ceases to prolong electromigration lifetimes. The critical extension length is a function of void size and electrical field gradient. The analytical model agrees very well with existing experimental results. Some design guidelines for electromigration-resistant circuits could be generated by the model.

I. INTRODUCTION

It is well known that the interfacial diffusion at Cu/SiN_x interface adversely contributes to the electromigration (EM) lifetime in Cu interconnects as opposed to grain-boundary diffusion in Al alloy conductors.[1,2] The in situ scanning electron microscopy (SEM) observations of upper and lower layer dual-damascene structures indicated that voids heterogeneously nucleate in the Cu/SiN_x interface at locations far from the cathode, move along the Cu/SiN_x interface in opposite direction of electron flow, and eventually agglomerate at the cathode end above the via prior to subsequent growth leading to eventual failure at the via.[3–5]

Considerable attention has been paid to modify this interface to improve EM lifetime. Some used different cap materials,[6–8] whereas the others proposed different process treatments before the deposition of the dielectric cap.[9,10] Embedded Ta into the Cu layer was also proven to block voids from propagating into the via and thus improved EM lifetime.[11] Another good choice to delay the EM failure is to introduce an extension (also described as overhang or reservoir) in the interconnects,[12] which serves as a reservoir for void growth, thus prolonging the median time to failure (MTTF). Recently, the reservoir effect in Al-Cu interconnect with W vias was reported,[13,14] where voids generally initiated at the W/Al interface by large Al atomic flux divergence. Lower levels of stress and vacancy concentration in the longer reservoir were proposed to contribute to the better EM reliability of interconnects. However, the reservoir mechanism in dual-damascene Cu interconnects is clearly different from that in W/Al via structures. Considering the technological importance of dual-damascene Cu interconnects, this work investigated the reservoir effect on EM lifetimes in Cu dual-damascene interconnects through analytical modeling. The obtained results were verified with experimental data.

II. MODELING

Real EM test specimens consisting of M1 and M2 via-fed structures (Fig. 1) were modeled. Experimental details are given elsewhere,[15] but the key test parameters and results are highlighted here. Cu deposition in the oxide trenches was performed by sputtering a 25 nm Ta barrier layer and a 150 nm Cu seed layer followed by Cu electroplating. SiN_x of 50 nm thick was used as a dielectric-cap layer. The test lines (M2) were 350 nm thick, 500 μm long, and 280 nm wide. The via diameter was 260 nm. M2 structures with extensions of 0, 60, and 120 nm were tested at 300 °C with a current density of 1.2 MA/cm^2. In each case, 12 samples were tested. It was

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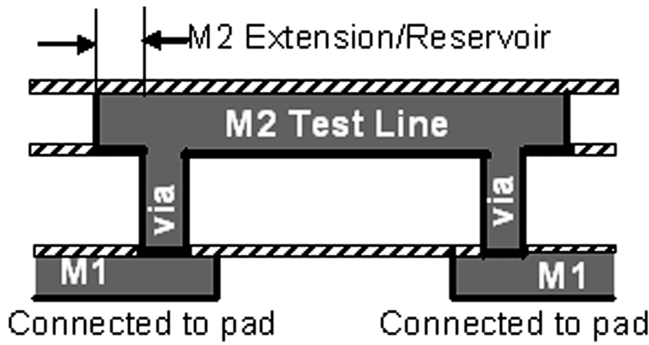

FIG. 1. Schematic cross section of M2-Via test structure.

found that for samples without extension, MTTF was about 60 h. MTTF was doubled in case of 60 nm extension. However, as the extension length was further increased from 60 to 120 nm, electromigration lifetimes did not show significant further improvement. It is thus proposed from the experiment, that there is a critical extension length (L_{crit}) beyond which increasing extension lengths ceases to prolong EM lifetimes.

The existence of L_{crit} will be characterized by an analytical model described later in this article. It is noted that the void migration process followed the same as the in situ SEM observation[3] that voids move along the Cu/SiN_x interface with the direction of current flow, and accumulate near the reservoir (Fig. 2).

A rectangular parallelepiped void ($2r \times 2r \times 2h$ in size) (inset in Fig. 2) centered at (x_c, y_c) of the 2D cross section (Fig. 2) was considered in the analytical model, where $x_c < 0$, $y_c = h$. The width of the void (i.e., size in the third dimension) is assumed to be the same as the length. The parameters describing the void are aspect ratio ($\varphi = h/r$) and volume ($V = 8r^2h$). Therefore, the dimensions in length and depth directions are expressed in terms of φ and V: $r = 0.5V^{1/3}\varphi^{-1/3}$; $h = 0.5V^{1/3}\varphi^{2/3}$.

Finite element modeling (FEM) demonstrates that the spatial distribution of x- and y-projections of electric field in the vicinity of void can be well approximated by

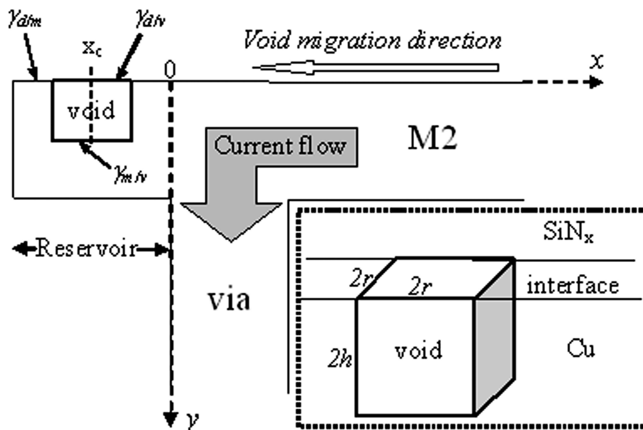

FIG. 2. Schematic of the void located at the overhang of M2 (dimensions not to scale).

simple polynomial dependencies including only first and second orders. In the current work, the electrical field in length (x-) direction is given by $-E_x(x, y = 0) \cong E_{\min} + \alpha(x_c)[x - (x_c - r)]$, where $x_c - r \leqslant x \leqslant x_c + r$, and E_{min} is the electrical field at the left edge of the void, assumed to be 0 in the present study. $\alpha(x_c)$ is the gradient of the electrical field in x-direction expressed as a second order polynomial function of the void centered location, x_c. Similarly, the electrical field in depth (y-) direction is expressed by $E_y(x,y) \cong \beta(x)\cdot y$, where $0 \leqslant y \leqslant 2h$, where $\beta(x)$ is the corresponding polynomial along y-axis. The electrical potential distribution in the void could be expressed as

$$\phi_{el} = -\left[\int_0^x E_x(x', y = 0)\,dx' + \int_0^y E_y(x, y')\,dy'\right] = \alpha(x_c)\,\frac{[x - (x_c - r)]^2}{2} - \beta(x)\cdot\frac{y^2}{2} \quad , \tag{1}$$

The total energy W of the system includes the electrical energy (W_{el}) and surface energy (W_{surf}), in

$$W = W_{el} + W_{surf} \quad . \tag{2}$$

And the electrical energy of the system is given by

$$W_{el} = W_{el}^{total} - W_{el}^{atoms\ in\ void} \quad , \tag{3}$$

where W_{el}^{total} is a constant, which is the electric energy of the whole sample without void; and $W_{el}^{atoms\ in\ void}$ is the energy of atoms if they would fill the void [i.e., the integral of the electrical potential from Eq. (1)]

$$W_{el}^{atoms\ in\ void} = -Z_v e \int_{xc-r}^{xc+r} \int_0^{2h} \int_0^{2r} \frac{dxdydz}{\Omega}\cdot\phi_{el}(x, y, z) \quad , \tag{4}$$

where Ω is atomic volume.

Surface/interface energy of the whole system is given by

$$W_{surf} = \gamma_{d/m}\cdot(S^{total} - 4r^2) + \gamma_{d/v}\cdot 4r^2 + \gamma_{m/v}\cdot(4r^2 + 16rh) = const + V^{2/3}\cdot\{\varphi^{-2/3}\cdot\Delta\gamma + 4\cdot\varphi^{1/3}\cdot\gamma_{m/v}\} \quad , \tag{5}$$

where S^{total} is the total area of the dielectric/metal interface without voids, $\gamma_{d/m}$, $\gamma_{d/v}$, and $\gamma_{m/v}$ are energies for dielectric/metal, dielectric vacuum, and metal/vacuum interfaces, respectively (Fig. 2). The difference in the energies is a fixed value: $\gamma_{d/v} + \gamma_{m/v} - \gamma_{d/m} \equiv \Delta\gamma$.

By combining Eqs. (3)–(5), the total energy of the system with void is obtained

$$W(\varphi, x_c, V)^{total} = const - V^{5/3}\cdot\frac{Z_v e}{6\Omega}\cdot\beta(x_c)\cdot\varphi^{4/3} + 4\cdot\gamma_{m/v}\cdot V^{2/3}\varphi^{1/3} + \left[\Delta\gamma\cdot V^{2/3} + V^{5/3}\cdot\frac{Z_v e}{6\Omega}\cdot\alpha(x_c)\right]\cdot\varphi^{-2/3} \quad . \tag{6}$$

To find the metastable shape of the void, we take $\partial W/\partial\varphi = 0$, from which

$$\frac{1}{3}\frac{Z_v eV}{\Omega\gamma_{m/v}}\cdot\beta(x_c)\cdot\varphi^2 - 2\varphi + \left[\frac{\Delta\gamma}{\gamma_{m/v}} + \frac{Z_v eV}{6\Omega\gamma_{m/v}}\cdot\alpha(x_c)\right] = 0 \quad . \tag{7}$$

Therefore, the optimized aspect ratio (φ) is a function of the void location (x_c) and void volume (V)

$$\varphi_{opt}(x_c, V) = \frac{\dfrac{\Delta\gamma}{\gamma_{m/v}} + \dfrac{Z_v eV}{6\Omega\gamma_{m/v}}\cdot\alpha(x_c)}{1 + \sqrt{1 - \left[\dfrac{1}{3}\dfrac{Z_v eV}{\Omega\gamma_{m/v}}\cdot\beta(x_c)\right]\left[\dfrac{\Delta\gamma}{\gamma_{m/v}} + \dfrac{Z_v eV}{6\Omega\gamma_{m/v}}\cdot\alpha(x_c)\right]}} \quad . \tag{8}$$

III. RESULTS AND DISCUSSION

To estimate the void aspect ratio, the following values for Cu are used: $Z_v e = 4e$; $\Omega = 1.66 \times 10^{-29}$ m^3/atom.[16] $\alpha(x_c)$ and $\beta(x_c)$ are about 10^8 V/m^2 based on our finite element analysis. Void volume is 10^{-22} m^3 for a $100 \times 20 \times 50$ nm void. The $\gamma_{m/v}$ value of Cu at the testing temperature (i.e., 300 °C) is unavailable. However, an estimation could be made according to the surface tension of molten copper, ~1.3 J/m^2 (Ref. 17); $\gamma_{d/v}$ value of Si_3N_4 at 1000 °C is equivalent to molten Cu[18]; $\Delta\gamma/\gamma_{m/v} < 1$ is expected due to the larger surface tension for the Cu/dielectric interface ($\gamma_{d/m}$). Based on these values, Eq. (8) is simplified as

$$\varphi_{opt}(x_c, V) \approx \frac{\dfrac{\Delta\gamma}{\gamma_{m/v}}}{1 + \sqrt{1 - \left[10^{-12}\cdot\beta(x_c)\cdot\dfrac{\Delta\gamma}{\gamma_{m/v}}\right]}} \approx 0.5 \times \frac{\Delta\gamma}{\gamma_{m/v}} < 0.5 \quad . \tag{8a}$$

It predicts that the void will be much wider in length (x-) direction, which is consistent with the in situ SEM observation where the voids were observed spanning along the Cu/dielectric interface.[3]

A discussion for the total system energy given by Eq. (6) is needed. The above optimized φ in Eq. (8) corresponds to the trapping situation shown in Fig. 3(a), in which the void volume should be less than certain critical value (V_{crit}), and the discriminant of the quadratic equation [Eq. (7)] is positive. However, if the void volume increases (e.g., due to the void accumulation), the discriminant will be negative. Thus, Eq. (7) has no real roots. This means that the energy [Eq. (6)] monotonically

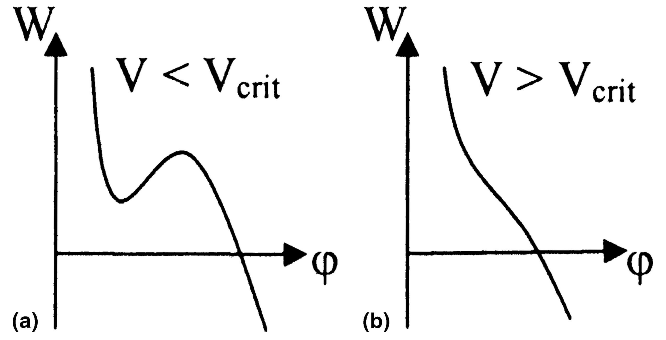

FIG. 3. Two possible energy (W) versus shape factor (φ) curves for Eq. (6), corresponding to (a) void trapping and (b) void de-trapping.

decreases with increasing shape factor [Fig. 3(b)]. Therefore, for sufficiently large void (V > V_{crit}) and/or sufficiently large current the void will start irreversible elongation toward via (void de-trapping), leading to fast failure. For the parameters used in the previous calculation, this effect is not noticed. However, if V is taken 1000 times larger (linear dimension about 10 times larger) and/or larger current density is assumed, the void de-trapping will be predicted, corresponding to the abrupt resistance increase of metallization during EM testing.[3]

With the optimized φ in Eq. (8), Eq. (6) could be re-arranged as

$$W(x_c, V)^{total} = const + \Psi(\varphi_{opt}(x_c, V), x_c, V) \quad , \tag{9}$$

and its derivative with respect to x_c

$$\frac{\partial}{\partial x_c} W(x_c, V) = [\alpha_1\cdot\varphi_{opt}^{-2/3}(x_c, V) - \beta_1\cdot\varphi_{opt}^{4/3}(x_c, V)] \cdot V^{5/3}\cdot\frac{Z_v e}{6\Omega} + \frac{\partial\Psi}{\partial\varphi}\cdot\frac{\partial\varphi_{opt}}{\partial x_c} \quad , \tag{10}$$

where $\alpha_1 = d\alpha(x_c)/dx_c$ $(= 2\alpha_{11}x_c + \alpha_{10})$; and $\beta_1 = d\beta(x_c)/dx_c (= 2\beta_{11}x_c + \beta_{10})$.

It is noted that $\partial\Psi/\partial\varphi = 0$ since φ is already optimized. To find the location for void trapping, we take $\partial W/\partial x_c = 0$, which gives a simple solution of

$$\frac{\beta_1}{\alpha_1} = \frac{1}{\varphi^2} \quad . \tag{11}$$

The salient point of this simple expression is that the void trapping location (x_c) could be extracted based on the electrical field gradients (i.e., α_1, β_1), and void aspect ratio φ. It is noted that α_1 and β_1 depend on current density and metal line dimensions, which can be evaluated by FEM. In the present study, a commercial package ANSYS (Canonsburg, PA) was used for the electrical field calculation. Eight-node, coupled field 3D elements SOLID5 were used in the calculation. The element size around the void is as fine as 5 nm. The calculated electrical fields along x-axis and y-axis, $\alpha(x_c)$ and $\beta(x_c)$ were,

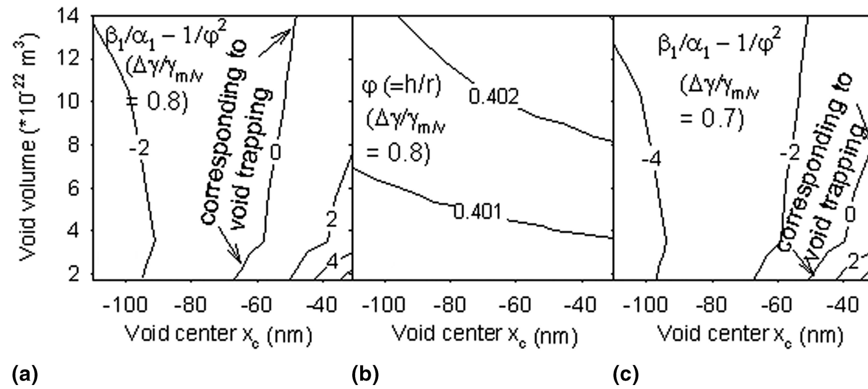

FIG. 4. Contours of (a) $\beta_1/\alpha_1 - 1/\varphi^2$ and (b) φ in terms of void volume and void center, where $\Delta\gamma/\gamma_{m/v}$ is assumed to be 0.8. (c) Contour of $\beta_1/\alpha_1 - 1/\varphi^2$ for $\Delta\gamma/\gamma_{m/v} = 0.7$.

respectively, curve-fitted with second order polynomials as described earlier. Their derivatives, α_1 and β_1, could then be obtained. One example of the calculation is shown in Fig. 4 for the test structure in Fig. 1 with 120 nm extension and current density 1.2 MA/cm^2. Figure 4(a) presents the contour of $\beta_1/\alpha_1 - 1/\varphi^2$ in terms of void volume and void center, where $\Delta\gamma/\gamma_{m/v}$ is assumed to be 0.8. As predicted by Eq. [8(a)], the corresponding aspect ratio φ is ~0.4 [Fig. 4(b)]. The location corresponding to the void trapping can be identified [Fig. 4(a)]. It is clearly seen that a void will migrate into the overhang, however, and be trapped ~60 nm left to the via. The void will stay there, and its size will increase only when another void moving along the Cu/SiN_x interface joins it. Figure 4(a) shows that a larger void will be drawn back slightly toward the via. It is also clear that φ increases with V increase [Fig. 4(b)], indicating that the void will extend to the via direction if its size is larger. Furthermore, when the void is large enough, it will irreversibly elongate toward via [Fig. 3(b)], favoring the metallization failure. The previously mentioned critical extension length (L_{crit}) could be characterized as the location corresponding to the void trapping (i.e., ~60 nm). If the extension length is larger than L_{crit}, no further prolonging EM lifetimes will be appreciated, agreeing well with the experiments.[15]

Figure 4(c) shows a contour plot of $\beta_1/\alpha_1 - 1/\varphi^2$ with a smaller $\Delta\gamma/\gamma_{m/v}$ value compared with Fig. 4(a). Clearly, with decreasing $\Delta\gamma/\gamma_{m/v}$, the void will be trapped closer to the via, indicating that L_{crit} is shorter. Physically this implies that the benefit provided by the reservoir will be greater if the Cu/dielectric interfacial energy ($\gamma_{d/m}$) could be reduced (i.e., $\Delta\gamma$ is increased). Separately, modification of the Cu/SiN_x interface[6–10] has been proven to improve the EM lifetime attributed to reduction of the interfacial energy. Based on the current model, we propose to use combined surface treatment and reservoir design, which should be able to enhance EM reliability further.

As given by Eq. [8(a)], φ is always <0.5, $\beta_1 > 4\alpha_1$ should be satisfied to meet the requirement from

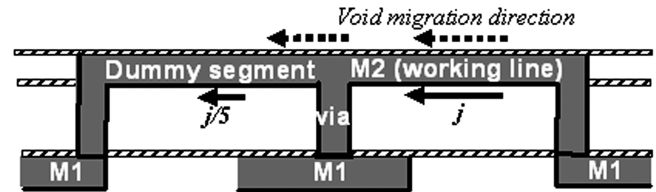

FIG. 5. Schematic of interconnect tree and current configuration, where the void along the Cu/SiN_x interface will move toward the dummy segment and thus prolong EM lifetime. The solid arrows show the current directions.

Eq. (11). In other words, the prerequisite to favor the void to continuously migrate into the overhang is that the gradient of the electrical field in y-direction be less than four times of that in x-direction. A possible solution through metallization design is to use interconnect tree where a dummy segment is placed to the left of the working line (Fig. 5). This dummy line should have a current flowing in the same direction as the working segment, imposing a strong x-direction electrical field to the void over the via. Thus, the void over the via will further migrate into the dummy segment (or overhang with infinite length), rather than extend to the via. The effectiveness of using the dummy segment has been demonstrated by the in situ SEM observation[4] and EM test.[19]

IV. CONCLUSION

In summary, the void migration mechanism of the Cu dual-damascene interconnect with overhang could be described as follows. Firstly, a void nucleates at Cu/SiN_x interface away from via and gradually moves along Cu/SiN_x interface opposite to the electron flow direction. The void will eventually be trapped over the via slightly toward the overhang (~tens of nanometers). As more and more vacancies moving along Cu/SiN_x interface join the void, its volume increases. The grown void will shift toward the via in both length and depth directions (i.e., x_c

approaching 0, and φ increasing). This process continues until the void growth eventually collapses the M2/via interface, resulting in the line opening. A simple yet quantitative analytical equation is derived in the current work. The results shed some new light on the problem of void migration and trapping behavior around M2/via region. The results also provide important information to the circuit designers for reliability improvement of Cu dual-damascene interconnects.

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