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# *In situ* observation of electromigration-induced void migration in dual-damascene Cu interconnect structures

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(Received 3 February 2004; accepted 27 July 2004)

*In situ* electromigration experiments were carried out to study electromigration-induced failure in the upper and lower layers in dual-damascene Cu test structures. The observations revealed electromigration-induced void movement along the Cu/dielectric cap interface. It supports the premise that $Cu/Si_3N_4$ interface acts as the dominant electromigration path. However, the observed void nucleation occurs in the $Cu/Si_3N_4$ interface at locations which are far from the cathode, and void movement along the $Cu/Si_3N_4$ interface in opposite direction of electron flow eventually causes void agglomeration at the via in the cathode end. The different electromigration behaviors of the upper and lower layer dual-damascene structures are discussed. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1795978]

Electromigration in dual-damascene Cu interconnects is currently one of the most important reliability issues in microelectronic devices.[1] Although most of the studies have shown that the $Cu/Si_3N_4$ cap interface is the dominant electromigration path,[2–10] some have reported grain boundary diffusion to be dominant [11,12] and have interpreted electromigration in Cu interconnects by coupling grain boundary and interface diffusion.[13] Others have indicated that the Cu/liner interface is the fast electromigration path.[14,15] Moreover, contrasting electromigration behavior of upper and lower layer dual-damascene structure was found,[16] and the effect of line width and length on electromigration was determined.[17] Due to the technological importance of dual-damascene Cu interconnects, it is necessary to understand the exact electromigration mechanism in these structures. *In situ* electromigration characterizations using scanning electron microscopy (SEM) on cross sections that contain embedded upper and lower layer dual-damascene test structures were carried out in this study in order to understand the electromigration mechanism.

Electromigration test structures were fabricated using advanced 0.18 $\mu$m dual-damascene Cu/oxide technology. Cu deposition in the oxide trenches was performed by sputtering of a 25 nm Ta barrier layer and a 150 nm Cu seed layer followed by copper electroplating. $Si_3N_4$ of thickness 50 nm was used as a dielectric-cap layer. Schematic representations of upper and lower layer test structures are depicted in Figs. 1(a) and 1(b), respectively. The lines connected to pads were shorter and wider so that voids would be formed in the narrower and longer test lines in between the vias. In the upper-layer test structures, the line to be tested was in the upper metal layer (M-2) with a width of 0.28 $\mu$m, thickness of 0.35 $\mu$m, and length of 800 $\mu$m. The structure of the lower layer test structures shown in Fig. 1(b) was exactly opposite to the upper layer structures with the line to be tested in M-1.

The via diameter was 0.26 $\mu$m for both upper and lower layer structures. The dice containing these test structures were attached to a ceramic package and gold wire-bonding was employed for electrical connection of the bond-pads to the package leads.

Evolution of electromigration was observed by *in situ* SEM electromigration characterization technique.[18] In this technique, cross sections at the cathode-end via region were prepared by focused ion beam milling such that the test structure remained fully embedded with a passivation oxide thickness of approximately 50–100 nm, while at the same time it became possible to image it by SEM with reasonable image quality. Upper and lower layer test structures were stressed at 350 °C with a current density of 10 $MA/cm^2$. The cathode-end via region was continuously imaged by SEM and the resistance was simultaneously monitored.

Some frames of SEM secondary electron images of one of the M-1 structures at the cathode-via region at various time intervals during electromigration stressing as well as the resistance trace are shown in Figs. 2(a) and 2(b). The void

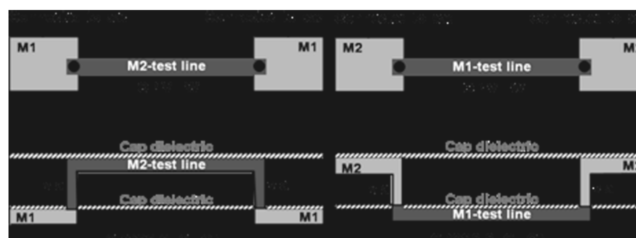


FIG. 1. Schematic of (a) upper (M-2) and (b) lower (M-1) layer test structure.

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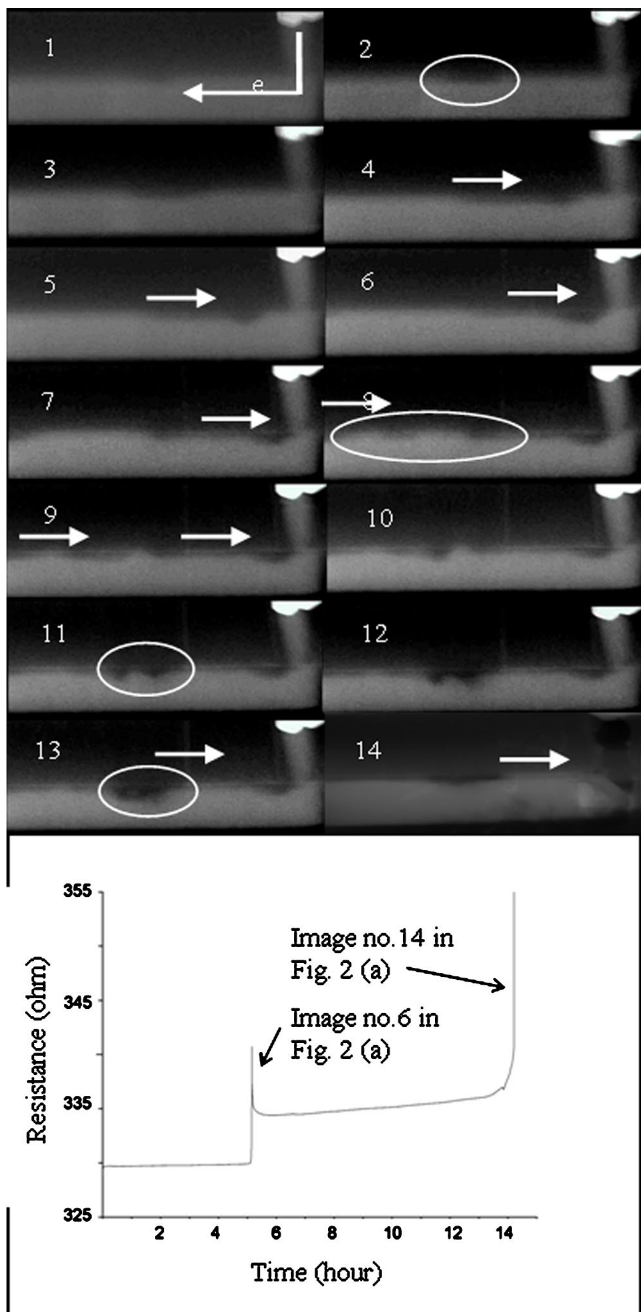


FIG. 2. (a) SEM of images of the cathode via region of M-1 test structure at various time intervals during *in situ* electromigration characterization (this particular M-1 structure was monitored for 14 h until failure occurred). (b) Resistance trace of the M-1 structure shown in (a).

first emerged at the $Cu/Si_3N_4$ interface at a considerable distance from the cathode via in the M-1 line and moved along this interface toward cathode end as shown in Fig. 2(a). The voids agglomerated near the via bottom along the $Cu/Si_3N_4$ interface leading to a sudden jump in resistance (as it can directly open the via), and finally grew further to cause opening of the entire via leading to via burn-out. Similarly, in the case of the M-2 structure, the void nucleated at the $Cu/Si_3N$ interface of the M-2 line at some distance from the via corner as shown in Fig. 3(a). The void agglomerated at the top corner of the M-2 line and its further growth toward the via caused an abrupt resistance increase. Over 20 samples were tested and all of them showed the same mechanism of void nucleation, movement, and agglomeration.

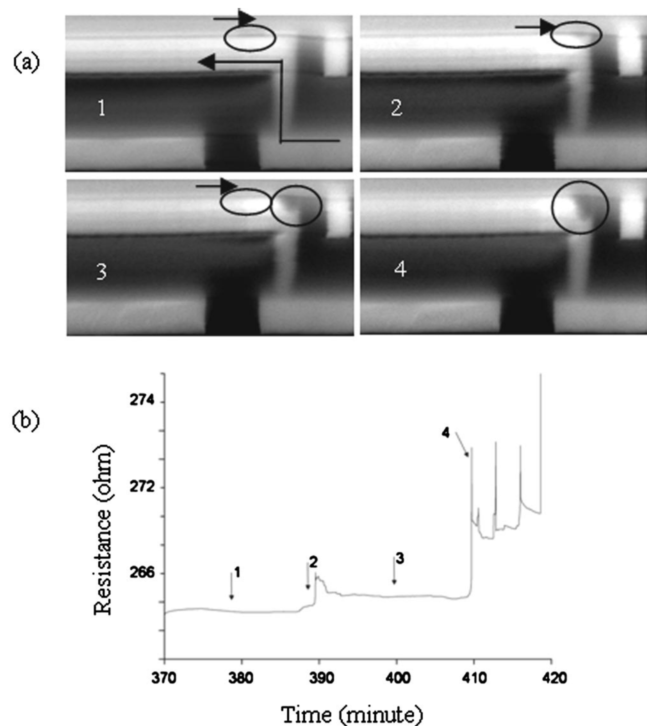


FIG. 3. (a) SEM of images of the cathode via region of M-2 test structure at various time intervals during *in situ* electromigration characterization (this particular M-2 structure was monitored for 7 h until failure occurred). (b) Resistance trace of the M-2 structure shown in (a).

The observed electromigration behavior supports the premise that the $Cu/Si_3N_4$ cap interface acts as the fast electromigration path,[2–10] but it contradicts previously proposed electromigration mechanisms in damascene interconnects.[3,16,19,20] The different electromigration behavior between M-1 structures and M-2 structures was proposed to be based on the location of maximum tensile stress developed during electromigration at the cathode end via bottom Ta barrier, which acted as the blocking boundary for Cu atom diffusion.[16] The void forms if the critical stress for void nucleation was reached. It was argued that in the case of M-2 structures the maximum tensile stress was reached at the base of the via where Cu was bounded by Ta on all sides whereas for the M-1 structure, the void nucleation site was thought to be at the Cu/dielectric cap interface near the via bottom due to the peak tensile stress which then grew along this interface. But this is contrary to the *in situ* observation shown in Fig. 2(a), which shows that the voids nucleated at the $Cu/Si_3N_4$ interface in the M-1 line, away from the via instead of the $Cu/Si_3N_4$ interface at the via. Subsequent to nucleation, the voids move along the $Cu/Si_3N_4$ interface, and agglomerated at the $Cu/Si_3N_4$ interface near the via bottom. It can be inferred from the *in situ* observations that the contrasting behavior of M-1 and M-2 structures is because of the structural differences. In both structures voids nucleate at the $Cu/Si_3N_4$ interface *away from the via* and *move* along the $Cu/Si_3N_4$ interface *in the direction opposite to electron flow*. But in the case of M-1 structure, the voids agglomerate directly below the via bottom in a high current density region, which can cause an electrical open quickly. It is interesting to note that in some reports,[2–5] voids were observed to be at $Cu/Si_3N_4$ interface *away from the via* for some of the samples, but these were ignored and not enough explanation is provided. Actually these voids must be the voids that were

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nucleated at the $Cu/Si_3N_4$ interface away from the via and moving toward the cathode end, according to our proposed mechanism.

It is interesting to consider here the recently proposed current crowding induced vacancy flux mechanism.[19] It proposed that the vacancy flux induced by electromigration goes from the high current density region to the low current density region. Accordingly, the void should nucleate at the bottom corner of the cathode end of M-1 line and at the top corner of the cathode end of M-2 line for the M-1 and M-2 structures, respectively. In our experiment, for the M-1 structure the void location at the Cu/dielectric cap interface is contrary to the void location expected by current crowding mechanism. The two possible explanations are that the highly resistive Ta liner has reduced the current crowding at the via interface,[21] and also while the proposed current density gradient force is large enough to drive a vacancy from the high to the low current density region, it is too small to drive a void. For M-2 structures although the final void location and shape are consistent with this mechanism, the void nucleation was actually at the Cu/dielectric cap interface at the line away from the cathode and the void aggregation at the top of cathode was due to void movement along this interface toward the cathode end. Owing to heterogeneous nucleation of a void on the Cu/dielectric cap interface, it requires only a small amount of supersaturation of vacancies to nucleate a void on the interface. For example, a triple point of Cu grain boundaries on the interface and the line intersection, where a Cu grain boundary meets the interface can become a heterogeneous site for void nucleation. So it can occur in the Cu/dielectric cap interface at locations which are away from the cathode in both the M-1 and M-2 structures.

The void movement can be understood based on the Cu atom transport along the periphery of the void, i.e., an inner surface, due to an electron wind force. This causes the void to move along the Cu/dielectric interface in the opposite direction to electron flow. Voids can grow by absorbing more vacancies and also voids can merge to form a larger void. We understand that theoretical studies on mechanism of void drift and coalescence are reported,[22–25] but this mechanism is not considered in the studies on electromigration in damascene structures.[2–7,16] Also, it should be noted that even Ho's theory of the drift of a single void[22] has not been tested satisfactorily.[23]

The condition for electromigration immortality due to the short strip effect in M-1 structures has been proposed to be the limit for void nucleation, and in M-2 structures, the proposed condition is when the electron wind force does not exceed the back-stress.[3] But the condition for M-1 structure may not be true here as it is assumed that the void should nucleate at the Cu/dielectric interface near the via bottom. Rather, the observations here suggest that the immortality condition for M-1 structure should also be similar to M-2 structure because the voids were found to nucleate at the Cu/dielectric cap interface in the line instead of near the via bottom. Overhang or extension above the via was found to improve the electromigration lifetime[20] as the void formed in these extensions delaying the via-opening. Our observations suggest that this technique may work for the M-2 type of structures, but may not work for the M-1 type of structures.

In summary, electromigration mechanism in dual-damascene Cu interconnect structures was revealed by *in situ* electromigration characterization using SEM. Void formation and migration on the Cu/dielectric interfaces have been observed. These findings have led to a better understanding of real electromigration mechanisms in dual-damascene Cu interconnects.


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