Direct evidence of electromigration failure mechanism in dual-damascene Cu interconnect tree structures

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In situ secondary electron microscope (SEM) characterizations were carried out to study electromigration failure mechanism in dual-damascene Cu interconnect tree structures, which are important for reliability assessment as well as design optimizations of on-chip interconnects. Direct evidence of electromigration-induced degradation in interconnect tree structure consisting of void nucleation and void movement in opposite direction to electron flow along the Cu/SiN_x interface was unraveled. The peculiar electromigration behavior of Cu interconnect tree structures can be clearly understood based on this mechanism. Dependence of electromigration mechanism of a segment in a Cu interconnect tree on current configuration in neighboring interconnect segment is discussed in detail. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2033136]

With continuous scaling of device dimensions, electromigration has become a severe reliability concern for integrated circuit (IC) interconnects. Although numerous studies on electromigration have been reported, most of them have employed straight via-to-via test lines or single layer lines directly connected to contacts. The interconnects in real ICs are much more complex with multiple interconnect line segments connected to vias. Interconnect tree structures are required for realistic electromigration studies which can correctly simulate the conditions in real onchip interconnects.[1] In-depth understanding of electromigration failure mechanism in interconnect tree structures is necessary for optimization of physical and electric design rules. Considering the design rules in future interconnect architectures, optimized onchip interconnect systems with high immunity to electromigration-induced failures will be designed. Electromigration studies on Al interconnect[1,2] and dual-damascene Cu interconnect[3,4] tree structures have been reported. Discrepancies in the behavior of Cu interconnect trees as compared to that of Al interconnect trees were observed, and it was found that in the case of Cu interconnect trees, the highest stressed tree segment is not always the least reliable.[3,4] As dual-damascene Cu interconnect technique is currently being employed for onchip interconnect fabrication, and will continue to be used for next technology generations in the near future due to significant cost advantage, it is of great technological significance to correctly understand the electromigration mechanism in dual-damascene Cu interconnect tree structures. In this letter, we report *in situ* observation of electromigration failure mechanism in Cu interconnect tree structures unraveled by *in situ* secondary electron microscope (SEM) characterizations, and its electromigration behavior is explained in detail.

Electromigration test structures were fabricated using advanced 0.18 μm dual-damascene Cu/oxide technology. The metallization stack consisted of sputtered (25 nm) Ta barrier layer and a (150 nm) Cu seed layer followed by electroplated Cu and finally (50 nm) plasma enhanced chemical vapor deposition (PECVD) SiN_x dielectric-cap deposited after Cu chemical mechanical polishing. Interconnect tree electromigration test structures consisted of 0.28 μm wide and 500 μm long straight via-to-via lines with an additional via in the middle of the line, same as the "dotted-I" interconnect tree structures in Refs. 3 and 4. The test lines were in the upper metal layer (M2), and bond pads were connected to wider connectors in the lower layer (M1) as shown in Fig. 1. The dice containing these test structures were attached to a ceramic package, and the bond-pads were connected to package leads by gold wire-bonding. Sample preparation for *in situ* SEM electromigration characterization was done by focused ion beam (FIB), details are described in Ref. 5. The interconnect tree structures were stressed at 300–350 °C with

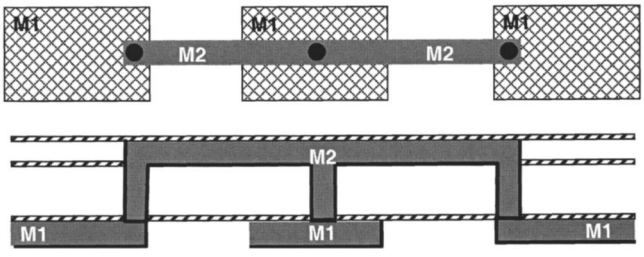

FIG. 1. Schematic of interconnect tree test structure.

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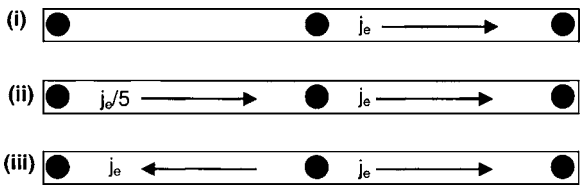

FIG. 2. Current configurations employed during *in situ* SEM characterizations (j_e=5 MA/cm^2–10 MA/cm^2 and arrows indicate electron flow direction).

various current configurations as explained in Fig. 2. Current density and direction in the right segment were kept constant while the left segment was stressed in various configurations. The middle via region was continuously imaged by SEM, and the resistance of the left and the right segments was simultaneously monitored. Sufficient number of samples were characterized to confirm consistency of the observed mechanism.

Some frames of SEM images of the middle via of an interconnect tree structure stressed in configuration (i) (no current in left segment) are shown in Fig. 3. The middle via region before starting electromigration stressing is shown in Fig. 3(a). Voids were observed to emerge at the Cu/SiN_x interface in the test line away from the via [Fig. 3(b)] and move towards the via in opposite direction to electron flow, consistent with our previous *in situ* electromigration studies on upper and lower layer dual-damascene Cu structures.[6] Cu atom transport along periphery of the void in direction of the electron flow (due to electron wind force) is responsible for the observed void movement opposite to electron flow direction. Hereafter, this mechanism will be referred as void movement in opposite direction to electron flow. Void movement and agglomeration at the middle via region was observed as shown in Figs. 3(c)-3(f). A void was formed at the Cu/SiN_x interface above the middle via and it moved slightly towards the left segment. However, the void neither moved further nor grew continuously. The void size was increased to span the via region only after agglomeration of additional voids moving along the Cu/SiN_x interface leading to failure of the right segment. The left segment of the interconnect tree also showed an open circuit after test. It is clear from these results why noncurrent carrying adjacent segments were observed to be open circuited during electromigration tests in other reported studies on Cu interconnect trees.[3,4] It should be noted that in this case there is no Cu/liner interface at the middle via region, which can provide a path for the void to sneak into the via as in case of standard upper layer structures.[5,6] So, the void cannot easily move into the via as in case of standard upper layer structures without any reservoir segment. The via opening is delayed because the void has to grow to a larger size by agglomeration of additional voids as compared to standard structures. Here, it is interesting to consider the current gradient induced vacancy flux effect.[7] This mechanism is also possible in these structures. However, the observations suggest that this mechanism is unlikely to play a dominant role in these test structures, at least during the initial stage of void evolution at via, because void was not found to be nucleated at low current density region.

The void agglomerated at the middle via region did not move further to the left in the case of configuration (i) because there was no current in the left segment to cause atom

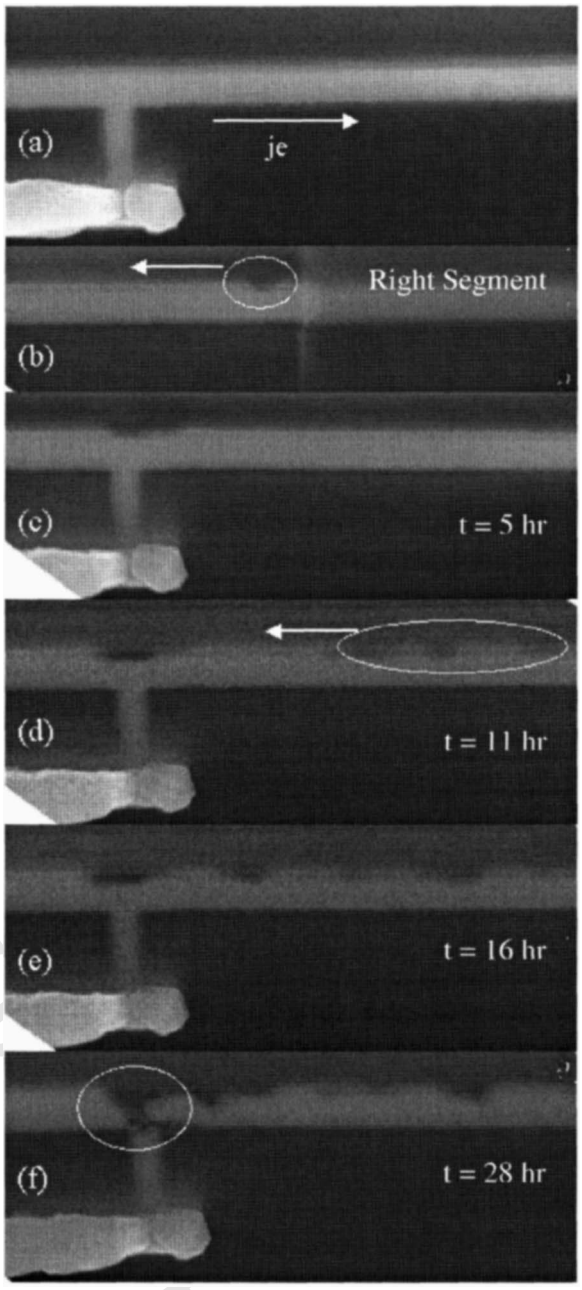

FIG. 3. SEM images of the middle via region at various time intervals for configuration (i).

transport along the void surface, which leads to void movement. However, if there is current flowing in the left segment in the same direction as the right segment, the void is expected to move further from via region into the left segment. Such mechanism was observed for interconnect tree structures with configuration (ii) as shown in Fig. 4. The voids

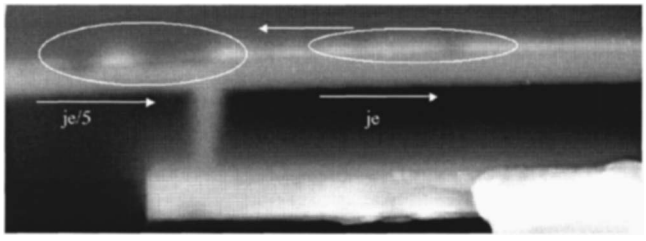

FIG. 4. SEM image of the middle via region for configuration (ii)

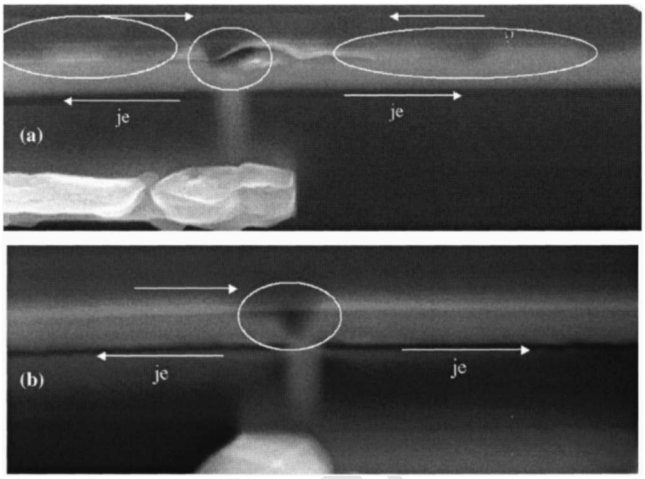

FIG. 5. SEM images of the middle via region for configuration (iii).

which agglomerated at the middle via region of the right segment moved further into the left segment. In this test, the left segment failed earlier than the right segment. This is because the void agglomeration at the middle via region (which is cathode end for the right segment) is averted by further void movement away from middle via into the left segment. It should be noted that the left segment failed earlier although it carried lower current density than the right segment. The previously reported experimental results on Cu interconnect tree suggesting that the highest current carrying segment may not be the least reliable[3,4] can be clearly understood based on the observed mechanism. Furthermore, as the current in the adjoining left segment was reversed, the voids moving along the Cu/SiN_x interface in both the segments converged at the middle via region as shown in Fig. 5(a). While for some samples, void from only one of the segments agglomerated at the middle via as shown in Fig. 5(b). This is due to statistical variation of time required for void nucleation and agglomeration in each of the segments. Interesting void shape evolution at middle via region was observed for these structures. This will be reported separately. The current understanding of electromigration mechanism in similar Cu interconnect tree structures is based on theory of maximum tensile stress developed in the middle via. The void is assumed to be nucleated at the liner in the middle via bottom, and then grow to span the via and interconnect segments.[3,4] The mechanism revealed by our *in situ* characterizations gives a much clearer understanding of the electromigration behavior of Cu interconnect tree structures. The sample size used in these experiments was not statistically significant to determine the relative electromigration performance dependence of the right segment based on current configuration in adjoining left segment. However, it can be easily inferred based on the observed mechanism that the configuration (iii) will have worst performance while the configuration (ii) will have better electromigration performance for the right segment. This inference is consistent with reported electromigration failure data of similar interconnect tree structures.[4]

In summary, the peculiar electromigration behavior of dual-damascene Cu interconnect tree structures is due to the electromigration mechanism, which involves void migration along Cu/SiN_x interface in a direction opposite to electron flow. These findings can be useful for an accurate assessment or prediction of circuit level electromigration reliability in complex onchip interconnect structures. The principle mechanism provided herein is only qualitative, a more complex physically based model[8] is necessary for quantitative assessment. Microstructure and current density distribution at the via need to be considered as they may play an important role during the final stage of electromigration-induced degradation, consisting of void evolution at the cathode via after agglomeration.

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